**Project 3 Evaluation**

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| Name: | | Total: | |
| Checklist | Weight | Earned | Notes |
| 1. Describe how you changed your C code and the architecture constraints to optimize your design. | 10 |  |  |
| 1. Write C testbench code to verify the function of your code and use Vitis HLS simulation tools to verify at this level. | 10 |  |  |
| 1. Describe your final choice of the constraint configurations and explain the advantages of your final design over the other trial designs that you made. | 10 |  |  |
| 1. Include and explain the timing scheduling results from the Vitis HLS Gannt chart schedule graphics. | 5 |  |  |
| 1. Give the timing and resource information from the synthesis and place and route implementation report from HDL Netlist generation after integration into Model Composer. | 10 |  |  |
| 1. Calculate maximum throughput of your system. | 5 |  |  |
| 1. Use Vitis HLS block to test the complete matrix multiplication in Model Composer as in Project 2. The design should support continuous matrix multiplication | 20 |  |  |
| 1. Do hardware in the loop Co-Simulation to verify performance of Vitis HLS code on the ZedBoard in the lab. | 10 |  |  |
| 1. Compare the results of this project with those from the Model Composer matrix multiplication project 2 and discuss the differences between the two design flows that possibly cause the different results. | 10 |  |  |
| 1. Turn in all project source files, .c, .m, .slx, and instructions on how to test. | 10 |  |  |